| Ref # | Hits | Search Query | DBs | Default Operator | Plurals | Time Stamp |
|---|---|---|---|---|---|---|
| L1 | 1345 | (nitrogen with (silicon adj oxynitride)) | US-PGPUB; USPAT | OR | ON | 2005/06/18 10:37 |
| L2 | 28 | 1 and (wafer with (test or dummy)) | US-PGPUB; USPAT | OR | ON | 2005/06/18 10:36 |
| L3 | 21 | 2 and (rapid or thermal) | US-PGPUB; USPAT | OR | ON | 2005/06/18 10:30 |
| L4 | 214 | (nitrogen with (silicon adj oxynitride)) | USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2005/06/18 10:36 |
| L5 | 1 | 4 and (wafer with (test or dummy)) | USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2005/06/18 10:36 |
| L6 | 0 | (monitoring or dertermining) with (nitrogen with (silicon adj oxynitride)) | US-PGPUB; USPAT | OR | ON | 2005/06/18 10:37 |
| L7 | 2 | (monitoring or dertermining) same (nitrogen with (silicon adj oxynitride)) | US-PGPUB; USPAT | OR | ON | 2005/06/18 10:39 |
| L8 | 1 | (monitoring or dertermining) same (nitrogen with (silicon adj oxynitride)) | USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2005/06/18 10:39 |

DOCUMENT-IDENTIFIER: US 20040235203 A1

TITLE: Monitoring of nitrided oxide gate dielectrics by determination of a wet etch

---------- KWIC ---------

Summary of Invention Paragraph - BSTX (8):

[0006] Other disadvantages associated with present processes stem from the fact that the **rapid** determination of changes in the nitrogen content of the gate oxides being fabricated in the production facility is not completely ideal. For instance, it is not optimally desirable to use the above-mentioned analytical methods to monitor and compensate for inadvertent drifts in the process used for nitridating gate oxides in a production environment due to the time factors mentioned above and the questionable impact on the quality of the nitrided gate oxide. It is also very difficult to monitor non-uniformities in the nitrogen content of the gate oxide formed across the surface of individual wafers in a production environment.

Brief Description of Drawings Paragraph - DRTX (6):

[0016] FIG. 4 presents exemplary data showing the relationship between etch rates of a nitrided oxide layer and plasma nitridation and **rapid thermal** anneal conditions used to form the nitrided oxide layer; and

Brief Description of Drawings Paragraph - DRTX (7):

[0017] FIG. 5 presents an exemplary nomogram showing the predicted change in thickness of nitrided oxide layers formed using different conditions of plasma nitridation and **rapid thermal** annealing under fixed etching conditions.

Detail Description Paragraph - DETX (2):

[0018] The present invention recognizes the advantages of using an etching process to monitor the nitridation of a gate oxide to provide more current quality data regarding the nitridation process. Certain embodiments make advantageous use of the present discovery that etch rates of silicon dioxide layers change as a function of certain process conditions used to nitridate the layer. For instance, while not limiting the scope of the invention by theory, it is believed that the extent of nitridation and **rapid thermal** annealing cause changes in the structure of the resulting silicon oxynitride that changes the

silicon oxynitride's properties, including its resistance to etching. By using carefully controlled etching conditions, it is possible to relate changes in the properties of the nitrided oxide layer to changes in the processing conditions used to nitridate the oxide layer.

Detail Description Paragraph - DETX (5):

[0021] In some preferred embodiments, the **test** substrate is a **test wafer** that is dedicated to monitoring the nitridation process. The **test wafer** is not further treated beyond the steps in the nitridation process as further described below. In an alternative embodiment, however, the **test** substrate comprises a portion of a semiconductor **wafer** used to form functional devices thereon. In such embodiments, substantially the same nitridation process is applied to other portions of the semiconductor wafer to manufacture integrated circuits.

Detail Description Paragraph - DETX (6):

[0022] Any conventional nitridation agent and process may be used to form the nitrided oxide dielectric layer. Suitable nitridation agents are molecular nitrogen (N.sub.2), ammonia (NH.sub.3), nitric oxide (NO), nitrous oxide (N.sub.2O) or other nitrogen sources well known to those skilled in the art. **Nitrogen** exposure may include the use of plasma, ion implantation, optical excitation, including laser excitation, or **thermal** processing to form **silicon oxynitride**. In some embodiments, the nitrided oxide dielectric layer is preferably formed by first thermally growing an oxide layer on a substrate and then nitridating the oxide layer.

Detail Description Paragraph - DETX (7):

[0023] In the various embodiments covered by the present invention, nitridation may be accomplished using a conventional plasma nitridation process. Examples include radio-frequency or microwave plasma nitridation processes. In some embodiments, the plasma nitridation process is carried out between about 5 and about 180 seconds, and more preferably between about 35 and about 55 second. Preferred conditions for plasma nitridation include a chamber pressure between about 10 mTorr and about 10 Torr, chamber temperature between about 20.degree. C. and about 500.degree. C., and plasma power between about 100 Watts and about 3000 Watts. In certain preferred embodiments, the RF plasma power range is between about 100 Watts and about 3000 Watts. In other preferred embodiments the microwave plasma power range is between about 600 Watts and about 3000 Watts. As discussed below with respect to an alternative embodiment, the nitridation process may be followed by a **rapid thermal** anneal (RTA).

Detail Description Paragraph - DETX (12):

[0028] The above-described optical spectroscopy procedures are also advantageous because they can be used to assess the uniformity of nitrided oxide dielectric layer across the surface of the test substrate. This is done by measuring the spectral characteristics of light reflected from a plurality of discrete locations of the test substrate. In certain embodiments of the method 100, for example, reflectance measurements are made, before and after the etch process, from 21 discrete locations on a **test wafer** substrate supporting the nitrided oxide dielectric layer.

Detail Description Paragraph - DETX (16):

[0032] FIG. 1B illustrates an alternative embodiment of the method 100 described above. In this exemplary embodiment, a test substrate is provided at step 140. The test substrate is preferably silicon, but can be any substrate suitable for integrated circuit construction. An oxide layer is formed on the test substrate at step 145. The oxide layer is preferably formed by thermally growing silicon dioxide to a desired thickness under conditions well known to those of ordinary skill in the art. In certain embodiments, for example, the oxide layer is less than about 30 Angstroms thick, and more preferably between about 10 and about 20 Angstroms thick. At step 150 the oxide layer is exposed to the nitridation process, as described above. However, in this embodiment, the nitridation process is preferably followed by a **rapid thermal** anneal (RTA), in step 155. The RTA functions to repair any surface defects formed during the plasma nitridation process. In some embodiments, the RTA comprises a temperature of between about 600.degree. C. and about 1000.degree. C. for between about 1 and about 60 seconds. At step 160, the previously described etch is conducted and the change in property value is conducted at step 165. A determination of whether the value is acceptable is then made at step 170. If no, at step 175, the nitridation process is modified and the process starts again at step 140. If yes, at step 185, the process is used to form a nitrided oxide layer on a production wafer.

Detail Description Paragraph - DETX (21):

[0037] In some preferred embodiments, the **test** sample 230 is located on a different **wafer** than the production substrate 240. In other embodiments, however, the **test** sample 230 is located on a **wafer** that also includes a production substrate 240. In such embodiments, the production substrate 240 can be subject to the above-described process of forming the nitrided oxide dielectric layer 215. The nitrided oxide dielectric layer 215 formed on the production substrate 240 is not subject to etch process, however. One skilled in the art would understand how to suitably prevent the production substrate 240 from being exposed to the etch process. For example, an etchant resistant

mask layer 245 is formed over the production substrate 240 when the test sample 230 is exposed to the etch process. The mask 245 is then removed before proceeding with additional manufacturing steps of the semiconductor device as further described below.

Detail Description Paragraph - DETX (30):

[0046] As illustrated in FIG. 3C, the process of manufacturing an integrated circuit 300 also includes forming one or more gate structures 325 on a production substrate 330. As previously discussed for other embodiments, the production substrate 330 may be located on the same or a different **wafer than the test** substrate 310. Forming the gate structure 325 includes forming a gate 335 on a production nitrided gate oxide layer 340. The production nitrided gate oxide layer 340 is formed using substantially the same oxide nitridation process as used to form the test layer 305, when the change in property of the test layer 305 as a function of the etch process falls within an accepted range, just discussed above with respect to FIGS. 3A and 3B.

Detail Description Paragraph - DETX (35):

[0050] Experiments were conducted to examine how nitridation affects the etch rate of an oxide layer. Layers of silicon dioxide were formed on silicon wafers to a thickness of about 25 Angstroms, using conventional **thermal** growth procedures. The thickness of the silicon dioxide layers were measured by conventional ellipsometry from 21 different locations on the wafer.

Detail Description Paragraph - DETX (36):

[0051] Individual wafers bearing the silicon dioxide layer were then exposed to predefined degrees of plasma nitridation and **rapid thermal** annealing. A conventional plasma nitridation process was performed. Plasma nitridation was carried out for either 0 (e.g., no plasma nitridation), or for between about 5 and about 180 seconds. Following plasma nitridation, a **rapid thermal** anneal (RTA) was performed on selected wafers at one of about 600.degree. C., about 800.degree. C. or about 1000.degree. C. The RTA was carried out for between about 5 and about 60 seconds. Other wafers were not thermally annealed. The wafers were then transferred to a wet etch chamber and exposed to identical buffered HF solutions (1:100 mixture of 49% wt./vol. HF to 41% wt./vol. NH.sub.3F) for different periods ranging from about 3 seconds to about 145 seconds, followed by conventional rinsing an drying procedures.

Claims Text - CLTX (15):

15. The process as recited in claim 9, wherein said forming said nitrided oxide dielectric layer includes performing a **rapid thermal** anneal after said nitridating.

US-PAT-NO: 6622059

DOCUMENT-IDENTIFIER: US 6622059 B1

TITLE: Automated process monitoring and analysis system for semiconductor processing

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Abstract Text - ABTX (1):

A method is provided for manufacturing, the method comprising processing a workpiece, measuring a parameter characteristic of the processing, and forming an output signal corresponding to the characteristic parameter measured by using the characteristic parameter measured as an input to a transistor model. The method also comprises predicting a **wafer** electrical **test** (WET) resulting value based on the output signal, detecting faulty processing based on the predicted WET resulting value, and correcting the faulty processing.

Brief Summary Text - BSTX (8):

However, traditional statistical process control (SPC) techniques are often inadequate to control precisely CDs and doping levels in semiconductor and microelectronic device manufacturing so as to optimize device performance and yield. Typically, SPC techniques set a target value, and a spread about the target value, for the CDs, doping levels, and/or overlay errors in photolithography. The SPC techniques then attempt to minimize the deviation from the target value without automatically adjusting and adapting the respective target values to optimize the semiconductor device performance, as measured by **wafer** electrical **test** (WET) measurement characteristics, for example, and/or to optimize the semiconductor device yield and throughput. Furthermore, blindly minimizing non-adaptive processing spreads about target values may not increase processing yield and throughput.

Brief Summary Text - BSTX (9):

Traditional control techniques are frequently ineffective in reducing off-target processing and in improving sort yields. For example, the **wafer** electrical **test** (WET) measurements are typically not performed on processed **wafers** until quite a long time after the **wafers** have been processed, sometimes not until weeks later. When one or more of the processing steps are producing resulting wafers that WET measurements indicate are unacceptable, causing the resulting wafers to be scrapped, this misprocessing goes undetected and

uncorrected for quite a while, often for weeks, leading to many scrapped wafers, much wasted material and decreased overall throughput. Similarly, process and/or tool problems throughout the wafer processing are typically not analyzed fast enough, and final wafer yields are not evaluated on a die-by-die basis. Furthermore, data sets for making correlations between processing and/or tool trace data, on the one hand, and testing data, such as WET measurements, on the other, are typically manually extracted by the process engineers and put together, a very time-consuming procedure.

Brief Summary Text - BSTX (12):

In one aspect of the present invention, a method is provided for manufacturing, the method comprising processing a workpiece, measuring a parameter characteristic of the processing, and forming an output signal corresponding to the characteristic parameter measured by using the characteristic parameter measured as an input to a transistor model. The method also comprises predicting a **wafer** electrical **test** (WET) resulting value based on the output signal, detecting faulty processing based on the predicted WET resulting value, and correcting the faulty processing.

Brief Summary Text - BSTX (13):

In another aspect of the present invention, a computer-readable, program storage device is provided, encoded with instructions that, when executed by a computer, perform a method for manufacturing a workpiece, the method comprising processing the workpiece, measuring a parameter characteristic of the processing, and forming an output signal corresponding to the characteristic parameter measured by using the characteristic parameter measured as an input to a transistor model. The method also comprises predicting a **wafer** electrical **test** (WET) resulting value based on the output signal, detecting faulty processing based on the predicted WET resulting value, and correcting the faulty processing.

Brief Summary Text - BSTX (14):

In yet another aspect of the present invention, a computer programmed to perform a method of manufacturing is provided, the method comprising processing a workpiece, measuring a parameter characteristic of the processing, and forming an output signal corresponding to the characteristic parameter measured by using the characteristic parameter measured as an input to a transistor model. The method also comprises predicting a **wafer** electrical **test** (WET) resulting value based on the output signal, detecting faulty processing based on the predicted WET resulting value, and correcting the faulty processing.

Detailed Description Text - DETX (6):

In various illustrative embodiments, there is further processing to do on the workpiece 100 (j<N) and the measuring step j 110 may involve a critical dimension (CD) measurement of a structure formed on the workpiece 100. FIG. 3 schematically illustrates the critical dimension (CD) measurement of a gate structure 300 formed on the workpiece 100. As shown in FIG. 3, a gate dielectric 310 for the gate structure 300 (for an MOS transistor 400 as shown in FIG. 4) may be formed above a structure layer 305, such as a semiconducting substrate (e.g., a silicon wafer). The gate dielectric 310 may be formed by a variety of known techniques for forming such layers, e.g., chemical vapor deposition (CVD), low-pressure CVD (LPCVD), plasma-enhanced CVD (PECVD), **thermal** growth (such as substrate oxidation in a furnace), and the like, and may have a thickness ranging from approximately 20-200 .ANG., for example. The gate dielectric 310 may be formed from a variety of dielectric materials and may, for example, be an oxide.(e.g., Ge oxide), a nitride (e.g, GaAs nitride), an oxynitride (e.g., GaP oxynitride), silicon dioxide (SiO.sub.2), a **nitrogen**-bearing oxide (e.g., **nitrogen**-bearing SiO.sub.2), a **nitrogen**-doped oxide (e.g., N.sub.2 -implanted SiO.sub.2), silicon nitride (Si.sub.3 N.sub.4), **silicon oxynitride** (Si.sub.x O.sub.y N.sub.z), and the like. In one illustrative embodiment, the gate dielectric 310 is comprised of a silicon dioxide (SiO.sub.2) having a thickness of approximately 50 .ANG., which is formed by an LPCVD process for higher throughput.

Detailed Description Text - DETX (11):

A titanium (Ti) metal layer (not shown) may have been blanket-deposited on the MOS transistor 400 and then subjected to an initial **rapid thermal** anneal (RTA) process performed at a temperature ranging from approximately 450-800.degree. C. for a time ranging from approximately 15-60 seconds. At surfaces 440 of active areas 445, such as the N.sup.+ -doped (P.sup.+ -doped) source/drain regions 420 and the doped-poly gate 310, exposed Si reacts upon heating with the Ti metal to form a titanium silicide (TiSi.sub.2) layer 435 the surfaces 440 of the active areas 445. The Ti metal is not believed to react with the dielectric spacers 425 upon heating. A wet chemical strip of the Ti metal removes excess, unreacted portions (not shown) of the Ti metal layer (not shown), leaving behind the self-aligned silicided (salicided) TiSi.sub.2 layer 435 only at and below the surfaces 440 of the active areas 445. The salicided TiSi.sub.2 435 may then be subjected to a final RTA process performed at a temperature ranging from approximately 800-1100.degree. C. for a time ranging from approximately 10-60 seconds.

Detailed Description Text - DETX (14):

As shown in FIG. 6, the output signal 125 is sent from the characteristic parameter modeling step 120 and delivered to a **wafer** electrical **test** (WET)

resulting value predicting step 130, producing at least one WET resulting value 145. In the WET resulting value predicting step 130, the characteristic parameter model may be used to predict one or more of the WET resulting value(s) 145 that would result if the semiconductor device and/or devices and/or process layers formed on the workpiece 100 were subjected to WET measurements in eventual WET steps performed later, sometimes weeks later. The WET may measure current and/or voltage responses of MOS transistors formed on the workpiece 100, for example, and/or capacitances and/or resistances of elements of MOS transistors formed on the workpiece 100.

Detailed Description Text - DETX (15):

For example, a WET measurement of a cobalt silicided (CoSi.sub.2) polysilicon serpentine structure (not shown) may be predicted, before the WET measurement is actually performed, by a characteristic parameter model with inputs from the relevant processing steps. The inputs from the relevant processing steps may comprise, but are not limited to, the critical dimension (CD) measurements of the width and thickness of the polysilicon of the cobalt silicided (CoSi.sub.2) polysilicon serpentine structure, the thickness of the cobalt (Co) deposited thereon, and parametrics associated with the **rapid thermal** annealing process used to form the cobalt silicide (CoSi.sub.2), such as the input power, measured temperature, and gas flows. Another example may be a WET measurement of transistor structure. In this case, the WET measurement may be a measurement of the drive current through a test transistor (like the MOS transistor 400, as shown in FIG. 4). This drive current measurement may be predicted by a characteristic parameter model, before the WET measurement is actually performed, using inputs from data gathered during the relevant processing steps. In this case, the inputs from the relevant processing steps may comprise, but are not limited to, implant dose and energies, critical dimension (CD) measurement of a poly gate conductive layer 315 thickness t.sub.p, spacer 425 width w.sub.s, silicide (such as TiSi.sub.2) 435 thickness t.sub.s, and/or a gate dielectric 310 thickness t.sub.ox, for example. The width W of the gate structure 300 may be related to the channel length L of the MOS transistor 400 as shown in FIG. 4.

Detailed Description Text - DETX (42):

Returning, to FIG. 10, once the characteristic parameter is identified and measured, the method 1000 proceeds by modeling the measured and identified characteristic parameter, using a **wafer** electrical **test** (WET) prediction model, as set forth in box 1030. The computer system 1130 in FIG. 11 is, in this particular embodiment, programmed to model the characteristic parameter. The manner in which this modeling occurs will be implementation specific.

Detailed Description Text - DETX (43):

In the embodiment of FIG. 11, a database 1135 stores a plurality of **wafer** electrical **test** (WET) prediction models that might potentially be applied, depending upon which characteristic parameter is measured. This particular embodiment, therefore, requires some a priori knowledge of the characteristic parameters that might be measured. The computer system 1130 then extracts an appropriate **wafer** electrical **test** (WET) prediction model from the database 1135 of potential models to apply to the measured characteristic parameters. If the database 1135 does not include an appropriate **wafer** electrical **test** (WET) prediction model, then the characteristic parameter may be ignored, or the computer system 1130 may attempt to develop one, if so programmed. The database 1135 may be stored on any kind of computer-readable, program storage medium, such as an optical disk 1140, a floppy disk 1145, or a hard disk drive (not shown) of the computer system 1130. The database 1135 may also be stored on a separate computer system (not shown) that interfaces with the computer system 1130.

Detailed Description Text - DETX (44):

Modeling of the measured characteristic parameter may be implemented differently in alternative embodiments. For instance, the computer system 1130 may be programmed using some form of artificial intelligence to analyze the sensor outputs and controller inputs to develop a **wafer** electrical **test** (WET) prediction model on-the-fly in a reaktime implementation. This approach might be a useful adjunct to the embodiment illustrated in FIG. 11, and discussed above, where characteristic parameters are measured and identified for which the database 1135 has no appropriate **wafer** electrical **test** (WET) prediction model.

Detailed Description Text - DETX (45):

The method 1000 of FIG. 10 then proceeds by applying the **wafer** electrical **test** (WET) prediction model to modify a MOSFET processing control input parameter, as set forth in box 1040. Depending on the implementation, applying the **wafer** electrical **test** (WET) prediction model may yield either a new value for the MOSFET processing control input parameter or a correction to the existing MOSFET processing control input parameter. The new MOSFET processing control input is then formulated from the value yielded by the **wafer** electrical **test** (WET) prediction model and is transmitted to the MOSFET processing tool controller 1115 over the line 1120. The MOSFET processing tool controller 1115 then controls subsequent MOSFET processing process operations in accordance with the new MOSFET processing control inputs.

Detailed Description Text - DETX (78):

Returning to FIG. 14, data preprocessing includes predicting the workpiece 1205 **wafer** electrical **test** (WET) measurement values that would be measured in a final **wafer** electrical **test** (WET) measurement step, using a **wafer** electrical **test** (WET) model, as set forth in box 1420. Known, potential characteristic parameters may be identified by characteristic data patterns or may be identified as known consequences of modifications to MOSFET processing control. For example, the identification and modeling of how changes in gate critical dimension affect the predicted final **wafer** electrical **test** (WET) measurements may fall into this latter category.

Claims Text - CLTX (1):

1. A method of manufacturing, the method comprising: processing a workpiece; measuring a parameter characteristic of the processing; forming an output signal corresponding to the characteristic parameter measured by using the characteristic parameter measured as an input to a partial least squares transistor model; predicting a **wafer** electrical **test** (WET) resulting value based on the output signal; detecting faulty processing based on the predicted WET resulting value; and correcting the faulty processing.

Claims Text - CLTX (25):

25. A computer-readable, program storage device encoded with instructions that, when executed by a computer, perform a method for manufacturing a workpiece, the method comprising: processing the workpiece; measuring a parameter characteristic of the processing performed on the workpiece; forming an output signal corresponding to the characteristic parameter measured by using the characteristic parameter measured as an input to a partial least squares transistor model; predicting a **wafer** electrical **test** (WET) resulting value based on the output signal; detecting faulty processing based on the predicted WET resulting value; and correcting the faulty processing.

Claims Text - CLTX (31):

31. A computer programmed to perform a method of manufacturing, the method comprising: processing a workpiece; measuring a parameter characteristic of the processing performed on the workpiece; forming an output signal corresponding to the characteristic parameter measured by using the characteristic parameter measured as an input to a partial least squares transistor model; predicting a **wafer** electrical **test** (WET) resulting value based on the output signal; detecting faulty processing based on the predicted WET resulting value; and correcting the faulty processing.

Claims Text - CLTX (37):

37. A method of manufacturing, the method comprising: forming a plurality

of structures on a workpiece using an in-line process metrology tool having at least one input value in a processing step; measuring a parameter characteristic of the plurality of structures; forming an output signal using the measured characteristic parameter and the at least one input value as inputs to a partial least squares transistor model; predicting a **wafer** electrical **test** (WET) resulting value based on the output signal; detecting faulty processing in the processing step based on the predicted WET resulting value; and correcting the faulty processing.